

**AMENDMENTS TO THE CLAIMS**

The listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A multi-processor system apparatus having a plurality of processors connected to each other by a network arrangement, comprising:

a multiplicity of processor elements, each processor element including a processor, a memory, and an interface for connection with said network arrangement; and

an array of multi-stage interconnection networks having a multiple stage connection arrangement where multiple stages of switching elements are provided for interconnection between said processor elements, wherein said processor elements and said multi-stage interconnection networks are grouped to clusters based on a specific number and arranged in multiple levels and the transfer of data packets between said processor elements is conducted according to a schedule statically determined with the use of switching state tables which are generated at different timings and indicate the status of the switching elements in said multi-stage interconnection networks, wherein

said multi-stage interconnection networks of a multiple stage connection arrangement are classified into two functions, an upstream linking network for upward transfer of data packets from the lower stage to the upper stage and a downstream linking network for downward transfer of data packets from the upper stage to the lower stage.

2. (Cancelled)

3. (Original) The multi-processor system apparatus according to claim 1, wherein said switching status table comprises data of a packet assigned to a particular output port, data of other packets demanding the connection to the output port, and data of the status of the output port of each switching element.

4. (Cancelled)

5. (Original) The multi-processor system apparatus according to claim 1, wherein when the connection to the output port of any switching element is demanded by two or more packets at the same timing, the transfer of packets between said processor elements is conducted as scheduled across said multi-stage interconnection networks so that a packet not assigned to the output port through a specific manner of arbitration is permitted to demand the output port with a switching status table at another timing.

6. (Cancelled)

7. (Original) The multi-processor system apparatus according to claim 5, wherein said multi-stage interconnection networks are of a cross connection arrangement and when the connection to the output port of any switching element is demanded by two or more packets at the same timing, the transfer of packets between said processor elements is conducted as scheduled across said multi-stage interconnection networks so that a packet not assigned to the output port through a specific manner of arbitration is permitted to demand another output port which is not demanded by other packets.

8. (Cancelled)

9. (Original) The multi-processor system apparatus according to claim 1, wherein the scheduling for each packet is preliminarily conducted by a compiler.

10. (Cancelled)